Cont F1

an ion implantation doped BST high dielectric constant thin film material having a substantially uniform stoichiometry formed over said at least two sidewall regions and over said second level;

wherein said ion implantation doped BST high dielectric thin film material is a continuous layer at least on said two sidewall regions and said second level.

41. (Second Amended) The capacitor according to claim 39, wherein said ion implantation doped BST thin film material is doped with a dopant selected from the group consisting of barium, strontium and titanium.

42. (Second Amended) The capacitor according to claim 39, wherein said ion implantation doped BST high dielectric thin film material is doped with a dopant selected from the group consisting of Ba and Sr.

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43. (Second Amended) The capacitor according to claim 39, wherein said ion implantation doped BST high dielectric thin film material is doped with Ti.

44. (Second Amended) The capacitor according to claim 43, wherein said ion implantation doped BST high dielectric thin film material contains a Ti percentage of from about 50% to about 53.5% throughout said BST high dielectric thin film material.

45. (Second Amended) The capacitor according to claim 44, wherein the ratio of Ba to Sr is about 70:30.

46. (Second Amended) The capacitor according to claim 39, wherein said ion implantation doped BST high dielectric thin film material is included in a DRAM cell.

48. (Fifth Amended) A capacitor comprising:

a material layer having a first level and a second level, said first and second levels being connected by at least two sidewall regions between said first and second levels; and

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an ion implantation doped doped BST high dielectric constant thin film material having a substantially uniform stoichiometry formed over said at least two sidewall regions and over said second level;

wherein said ion implantation doped BST high dielectric thin film material is a continuous layer at least on said two sidewall regions and said second level; and

a capping layer provided over at least a portion of said ion implantation doped BST thin film material.

50. (Second Amended) The capacitor according to claim 48, wherein said ion implantation doped BST thin film material is doped with a dopant selected from the group consisting of barium, strontium and titanium.

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51. (Second Amended) The capacitor according to claim 48, wherein said ion implantation doped BST high dielectric thin film material is doped with a dopant selected from the group consisting of Ba and Sr.

52. (Second Amended) The capacitor according to claim 48, wherein said ion implantation doped BST high dielectric thin film material is doped with Ti.

53. (Second Amended) The capacitor according to claim 52, wherein said ion implantation doped BST high dielectric thin film material contains a Ti percentage of from about 50% to about 53.5% throughout said BST high dielectric thin film material.

Cont F4

54. (Second Amended) The capacitor according to claim 53, wherein the ratio of Ba to Sr is about 70:30.

55. (Second Amended) The capacitor according to claim 48, wherein said ion implantation doped BST high dielectric thin film material is included in a DRAM cell.

74. (Fifth Amended) An integrated circuit capacitor device comprising:

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a first electrode having a first level and a second level, said first and second levels being connected by at least two sidewall regions between said first and second levels; and

an ion implantation doped BST high dielectric constant thin film material formed over said at least two sidewall regions and over said second level;

wherein said ion implantation doped BST high dielectric thin film material is a continuous layer at least on said two sidewall regions and said second level; and

a second electrode provided on said ion implantation doped BST high dielectric thin film material.